REMARKS

Examiner J. Diaz is thanked for a complete search and thorough Office Action.

Reconsideration of the rejection of claims 18-19 under 35 U.S.C. 102(e) as being anticipated by Saitou et al. (U.S. Patent 5,739,546), claim 20 under 35 U.S.C. 103(a) as being unpatentable over Saitou et al. (U.S. Patent 5,739,546) in view of Lou (U.S. Patent 5,759,906), and of claims 21-22 under 35 U.S.C. 103(a) as being unpatentable over Saitou et al. (U.S. patent 5,739,946) is respectfully requested for the following reasons.

Response dated September 5, 2002 to previous Office Action dated June 13, 2002 is still valid.

In reply to Examiner's Response to Arguments in the Final Office Action dated December 3, 2002, the Examiner states that the applicant argues that Saitou et al. do not teach a patterned fill layer. However, the Examiner disagrees.

To better appreciate the difference between the applicant's claimed structure and Saitou's claimed structure, the following comparison is provided.

In Saitou's patent, the integrated circuit is completely finished before he forms his burn-in test structure. Saitou's structure would not be used at a first

level of metal integration when several levels of metal integration are used to complete the wiring of the integrated circuit. Generally in current product fabrication of semiconductor integrated circuits, multilevels of metal integration are used to complete the wiring, as depicted in applicant's Fig. 8. Therefore, Saitou would not be motivated to use his burn-in test structure until the multi-levels of metal integration are used to complete the integrated circuit, as indicated in Saitou's col. 1, lines 44-53. Saitou is testing the integrated circuit, and is not using a test structure at each level of metal integration. One cannot do a burn-in test on a device unless the wiring is completed.

The applicant's claimed invention is a fill area at each level of metal integration, and one would not form a burn-in test structure until the integrated circuit is completed. Therefore, Saitou's structure would only be made on the top surface of applicant's claimed structure (see applicant's Fig. 7).

Another difference as shown in Saitou's Figs. 2-3 is that the burn-in test structure in the scribe line area (applicant's kerf area) is made up of a ground plane 6 and a power line 8, with an insulator 7 in between, and a protection layer 9 over the power line 8. Saitou is completely silent about using this structure as a fill layer in the scribe areas, as shown in Saitou's Figs. 9-10. The applicant forms a fill layer 12B from a single metal layer

(see applicant's Fig. 6-7), and for a multilevel metal structure the applicant uses a sequence of fill areas 12B, 22B, and 32B as shown in applicant's Fig. 8. Further, Saitou's Figs. 2, 3, 9, and 10 show insulating layer 7 and protective layer 9, which are not planar, and therefore he is not using the burn-in test structure as a fill structure to planarize a spin-on glass.

Although the process in a product-by-process claim holds no weight in the patentability of the final product, as pointed out by the Examiner, it should be apparent from the above description that the applicant's claimed structure is significantly different from the prior art.

The applicant's claimed structure is non-obvious and is patentable over the prior art of Saitou et al. and further in view of Lou.

It is requested that Examiner Jose R. Diaz call the undersigned Attorney at 845-452-5863 should there be anything that can be done to help bring this Patent Application to Allowance.

Respectfully submitted,

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